

Amendments to the Specification

Please replace the paragraphs on page 18, lines 2-19 with the following amended paragraph:

With reference to Fig. 1, as an example of clock generation circuit 1A in accordance with the first embodiment of the present invention, power supply potential VCC or ground potential GND may be changed only in at least one of buffer circuits 10-0A, 10-1A, 10-2A, 10-3A. In this case, as the logical threshold value of the buffer circuit is shifted, the duty ratio of the output buffer signal can be changed. It is noted that the duty ratio of the output buffer signal can be adjusted using a control signal (see Fig. 2, signals P11-P1n and N11-N1n) by adjusting the amount of change in power supply potential VCC or ground potential GND using the control signal.

With reference to Fig. 1, as another example of clock generation circuit 1A in accordance with the first embodiment of the present invention, a substrate potential of a transistor included in the buffer circuit may be changed only in at least one of buffer circuits 10-0A, 10-1A, 10-2A, 10-3A. In this case, as the logical threshold value of the buffer circuit is shifted, the duty ratio of the output buffer signal can be changed. It is noted that the duty ratio of the output buffer signal can be adjusted using a control signal (see Fig. 2, signals P21-P2n and N21-N2n) by adjusting the amount of change in substrate potential of the transistor using the control signal.